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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,841	10/08/2004	G. R. Mohan Rao	A4-1845	5840
27127	7590	06/28/2006	EXAMINER	
HARTMAN & HARTMAN, P.C. 552 EAST 700 NORTH VALPARAISO, IN 46383			LE, THONG QUOC	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

—A

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/711,841	RAO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4,7-14,17-27 is/are rejected.
- 7) ☒ Claim(s) 5,6,15 and 16 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____.  |

### **DETAILED ACTION**

1. Claims 1-27 are presented for examination.

#### ***Specification***

2. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### ***Claim Objections***

3. Regarding claims 2-10, 12-20, line 1, should be changed "A semiconductor" to –  
The semiconductor--.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4,7-14,17-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Delp et al. (Pub. U.S. Patent No. 2002/0013881).

Regarding claims 1, Delp et al. disclose a semiconductor memory device (Figure 5) comprising a bank with multiple pages (Figure 5, 74, [0047]), the device comprising means (Figure 7, 98a) for keeping multiple pages open on the bank ([0076]).

Regarding claims 2, Delp et al. disclose wherein the keeping means is operative to post a precharge command immediately after a command for a first access of one of

the multiple pages in anticipation of a subsequent access of the page, the keeping means keeping the page open for a number of clock cycles and the precharge command causing a precharge operation to be executed after completion of the number of clock cycles ([0076-0078]).

Regarding claims 3,13-14, Delp et al. disclose further comprising means (Figure 6, 94) for resetting the keeping means if the subsequent access of the page occurs while the page is open, the resetting means operating to further delay execution of the precharge operation initiated by the precharge command ([0073-0077]).

Regarding claim 4, Delp et al. disclose wherein the bank comprises memory cells arranged in arrays of rows and columns ([0047]), and the keeping means comprises a counter (Figure 7, 98a) in a row path operatively connected to the rows of the bank ([0097]).

Regarding claims 7, 17, Delp et al. disclose wherein bank comprises memory cells arranged in arrays of rows and columns the memory cells comprises storage cells, and the storage cells comprise at least one transistor and at least capacitor ([0064]).

Regarding claims 8,18, Delp et al. disclose wherein the device has a dynamic random access memory architecture ([0007]).

Regarding claims 9, 19, Delp et al. disclose wherein the device is nonvolatile memory device with multiple pages open in a block or sector ([0060]).

Regarding claims 10,20, Delp et al. disclose wherein the device is a flash memory device ([0046]).

Regarding claim 11, Delp et al. disclose a semiconductor memory controller (Figure 7, 82) operable to issue commands (Figure 7, CMD) to a memory module comprising multiple memory integrated circuits (Figure 5, 47) with memory cells arranged in arrays of rows and columns defining multiple pages, the memory controller comprising means for performing a posted precharge operation (Figure 7, 98) immediately after a command for a first access of a page in anticipation of a subsequent access of the page ([0076]).

Regarding claim 12, Delp et al. disclose wherein the performing means comprises a counter (Figure 7, 98a) in a row path operatively connected to the rows of the memory cells (Figure 7, Figure 5, 80).

Regarding claim 21, Delp et al. disclose a method comprising the step of keeping (Figure 7, 98a,b) open more than one page of multiple pages on a banks of semiconductor memory device ([0076]).

Regarding claim 22, Peld et al. disclose wherein the step comprises posting a precharge command immediately after a command for a first access of one of the multiple pages in anticipation of a subsequent access of the page ([0077]).

Regarding claim 23, Peld et al. disclose wherein the page is kept open for a number of clock cycles following the precharge command and the precharge command causes a precharge operation to be executed after completion of the number of clock cycles (Figure 10, ([0050], [0092-0095]).

Regarding claim 24, Delp et al. disclose the step of resetting the number of clock cycles if the subsequent access of the page occurs while the page is open, the resetting

step operating to further delay execution of the precharge operation (Figure 10, CLK, [0094], [0096]).

Regarding claim 25, Delp et al. disclose wherein a precharge operation is initiated the precharge command and following a delay determined by counter (0055-0057)).

Regarding claim 26, Delp et al. disclose the step of resetting the counter so as to further delay the precharge operation if the subsequent access of the page occurs while the page is open ([0057]).

Regarding claim 27, Delp et al. disclose wherein the bank comprises memory cells arranged in arrays of rows and columns (Figure 5, 74) , and the precharge command is performed by a precharge counter (figure 7, 104) that, when a row address is latched and a page is opened, the counter locks into the row address until reset, and when the precharge command is made, an internal activation (Figure 10, Activate CMD) for performing a precharge operation is activated after a predetermined number of clock cycles (Figure 10, [0092-0095]).

#### ***Allowable Subject Matter***

6. Claims 5-6,15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


Claims 5-6,15-16 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Delp et al. (Pub. U.S. Patent No. 2002/0013881), and others,

does not teach the claimed invention having latches coupled to sense amplifier associated with the bank, and the latches operating in storage of data read from and written-to the sense amplifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Thong Q. Le  
Primary Examiner  
Art Unit 2827

6/20/2006